CLAIMS:

1. A display device (2) with pixels (8) arranged in columns m and rows n, in which the pixels of a row n can be selected by means of a row voltage (V_{ROW}) supplied via control lines (6), and column voltages (V_{COL}) that correspond to the image data of the selected pixel (8) to be displayed can be supplied via data lines (7), wherein mutually adjoining pixel groups arranged in a row or column, consisting of adjoining pixels of a row or column, are connected to adjoining control lines (6n, 6n+1) or data lines (7n, 7n+1), as applicable, in alternation.

2. A display device as claimed in claim 1, characterized in that a pixel group comprises one pixel (8).

3. A display device as claimed in claim 1, characterized in that mutually adjoining pixels (S11, S12, S13, S14) of one row are alternately connected to the adjoining control lines (6n, 6n+1).

4. A display device as claimed in claim 3, characterized in that a delay unit (V) is connected to every second data line (Col_1, Col_3, Col_5), which unit is provided for storing column voltage values (V_{COL}), while a clock signal (CLOCK) can be supplied to the delay units.

5. A display device as claimed in claim 1, characterized in that mutually adjoining pixels (S11, S21, S31, S41) of a column are connected to the adjoining data lines (7m, 7m+1) in alternation.

6. A display device as claimed in claim 5, characterized in that a delay unit (V) is arranged in every second control line (6n, 6n+2), which unit is provided for storing row voltage values (V_{ROW}), while a clock signal (CLOCK) can be supplied to the delay units.

7. A display device as claimed in claim 1, characterized in that pixels comprise switching elements (S_{XX}) with control terminals (11) which are connected to control lines (6n, 6n+1, 6n+2) and data terminals (12) which are connected to data lines (7m, 7m+1, 7m+2).

8. A display device as claimed in claim 1, characterized in that the rows (n) and columns (m) situated at the edges of the display device are covered.

9. A method of controlling a display device as claimed in claim 4, wherein the column voltages (V_{COL}) for the columns (Col_2, Col_4, Col_6) are supplied to the pixels of the selected row without delay unit (V) upon the clock signal (CLOCKn), and the column voltage values (V_{col2}, V_{col4}, V_{col6}) stored in the delay units are supplied to the pixels of the selected row, and the column voltages applied to the data lines (Col_1, Col_3, Col_5) for the columns with the delay units are read into the delay units upon the clock signal and are stored therein until the next clock signal (CLOCKn+1).